Preliminary
ANX2684
Product Brief

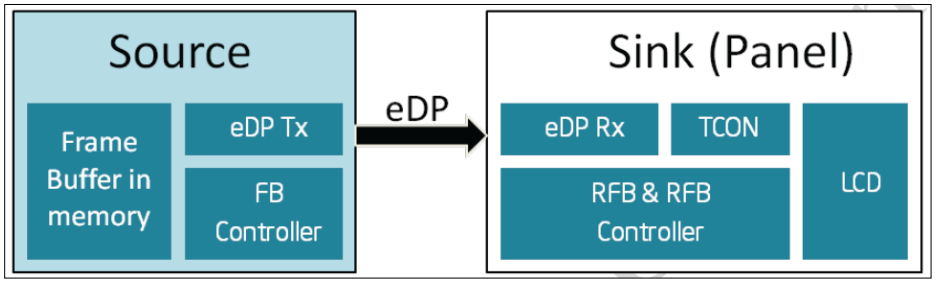
eDP 1.4a-compliant TCON with PSR and Selective Update PSR (PSR2)

The ANX2684 is an eDP 1.4a-compliant TCON with Panel Self Refresh (PSR) and Selective Update PSR (PSR2) functions. The ANX2684 features RapidLink™ and QuietLink™. The RapidLink feature allows for instantaneous clock recovery for no-link training wake-up and the QuietLink feature reduces DisplayPort voltage swing, which helps reducing power consumption. The ANX2684 has Analogix-patented low power consumption technology of Gapless architecture. It has stack LPDDR2 die inside package to support PSR and PSR2 feature. The DRAM size is 256M bits (4x64M). It also supports Instant-on feature. Figure 1 1 shows the system block diagram of the eDP TCON chip...

Features

- Resolution supported: up to 3240 x 2160 display resolution; color depth supported: 18/24bpp (input), 24bpp (output)
- PSR/MBO/PSR2 function by 256Mb LPDDR2 stack die
- eDP receiver
  - Compliant with DisplayPort standard v1.3 and eDP standard v1.4a
  - Up to 4-lanes, 5.4Gbps, 4.32Gbps,3.24Gbps,2.7Gbps,2.16Gbps and 1.62Gbps for each port
  - Down-spread spectrum supported (0.5% down spread)
  - Alternate Scrambler Seed Reset (ASSR) for eDP Display Authentication and Content Protection
  - Normal/Fast/No link training
  - EDID access through AUX channel
  - Support eDP 1.4a panel functions
  - eDP 1.4a power sequence
  - Support DRRs/NvDRRs/SDRRs functions
- Adaptive Sync function and Direct Drive G-Sync.
- EPI protocol
  - Supports up to 16-channels with 1D/1C and up to 8-channels 2D/1C configuration.
  - EPI transmitter up to 1.54Gbps configuration
  - EPI PHY supports output swing level control
  - On-chip SSCG (Max. +/-1% with 0.25 step, 10/20/30/40KHz, center spreading)
  - Support various swap modes: inter-port swap, intra-port swap, P/N swap, RGB swap, Odd/Even pixel swap etc.
  - Support Scan direction swap
  - Support Dual CTR1 package iteration
  - Support 5 types of POL polarity control method
  - 1-6 frame POL for LRR MBO
  - Z-inversion(column inversion),and N-line inversion
  - Programmable charge share control including disable
  - EPI test pattern mode
- iSP protocol
  - Support up to 8-channel 2D/1C or 1D/1C configuration.
  - iSP transmitter up to 1.62Gbps configuration
  - iSP PHY support output swing level control
  - iSP output support +/- 1% spread-spectrum clocking
  - Support various swap modes: inter-port swap, intra-port swap, p/n swap, RGB swap, odd/even pixel swap etc.
  - Support Scan direction swap
  - Support Z-inversion(column inversion),and N-line inversion
  - Support iSP test pattern mode
- TCON function
  - Support Gate D-IC /GIP/Overlap Driving/Multi Driving/4,6,8 phase simple GIP through GPIO
  - Power-up gate output masking to avoid DC/DC over-loading
  - Programmable Fail-safe mode control
  - Configurable BIST pattern
  - Support various FRC pattern configurations
  - Support 10bit->8bit, 10bit->6bit, 8bit->6bit, and 9bit->6bit FRC modes
  - Support LGD LRR Sharp LRD function
- Instant-on feature
- Communication Interface
  - I2C Master for EEPROM loading, support the Fast-mode, typical the bit rate at 330 kbit/s
  - I2C Slave #1(SN_SCL, SN_SDA) and I2C Slave #2(ARC_SCL, ARC_SDA), up to 1Mbit/s speed
  - I2C Slave #1 share pinout with SPI Slave
  - I2C Slave #2 share pinout with TCON I2C Slave
  - SPI Slave: up to 50MHz
  - JTAG for debugging

- LC frequency: 27M±300KHz (with eFuse applied)
- Clock spreading on DDR interface to suppress EMI
- Support Video BIST, SRAM BIST and video CRC check
- EEPROM shared for EDID and panel configuration
- Support shadow EDID inside TCON
- EDID and configuration content check-sum support, and support CRC32 check for Instant On PNG data
- RapidLink provided
- QuietLink provided
- Pin-to-pin compatible with ANX2604
- UMC 55nm process
- Power supply: 1.8V/1.25V/1.0V (3.3V generated internally for HPD output)
- Package: 144-pin BGA (8x18); package size: 5.5×12×1.0mm (W×L×H)
- Power consumption (estimated)
  - 480mW, with PSR enabled and at the resolution of 2736 × 1824, 8-bit color depth
  - 550mW, with PSR disabled and at the resolution of 2736 × 1824, 8-bit color depth
  - 680mW, at the maximum usage and the resolution of 3240 × 2160, 8-bit color depth



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